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February 18, 2004

Commissioner for Patents P.O.Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/724,784 12/01/03

May-Ho Ko

FLASH PROCESS FOR STACKING POLY ETCHING

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February ? }, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Signature/Date

TSMC-00-932

U.S. Patent 6,165,375 to Yang et al., "Plasma Etching Method," discloses a flash step in an etch process.

U.S. Patent 6,165,861 to Liu et al., "Integrated Circuit Polysilicon Resistor Having a Silicide Extension to Achieve 100% Metal Shielding from Hydrogen Intrusion," discloses a method for a mixed mode product.

The following two U.S. Patents discloses processes for mixed mode products using poly etches:

- 1) U.S. Patent 6,103,622 to Huang, "Silicide Process for Mixed Mode Product with Dual Layer Capacitor and Polysilicon Resistor which is Protected with a Capacitor Protective Oxide During Silicidation of FET Device."
- 2) U.S. Patent 6,103,621 to Huang, "Silicide Process for Mixed Mode Product with Dual Layer Capacitor which is Protected by a Capacitor Protective Oxide During Silicidation of FET Device."

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Stephen B. Ackerman,

Reg. No. 37761

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